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For: LIQUID CRYSTAL DISPLAY WITH
NOTCHED GATE LINE AND GATE
ELECTRODE (AS AMENDED)

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Herein submitted is a Certified Translation of Korean Patent Application 2002-0087770, filed December 31, 2002.

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CERTIFICATION THAT TRANSLATION IS TRUE AND ACCURATE

I, SU HYUN LEE, state that the translation
attached hereto is a true and accurate translation of the attached Korean Patent
application, 2002-0087770, filed December 31, 2002.

Date: 17th day of May, 2006 Signature: _____

A handwritten signature in cursive script, appearing to read "Su Hyun Lee", written over a horizontal line.



[ABSTRACT OF THE DISCLOSURE]

02-87770

[ABSTRACT]

An LCD device and a method for manufacturing the same is disclosed, in which structures of a gate electrode and a gate line are changed, so that it is possible to prevent a data line and a drain electrode from being open at crossing areas (step difference) overlapped with the gate line and the gate electrode, respectively. Also, it is possible to prevent signal distortion by minimizing Cgd change. The LCD device includes a gate line arranged at one direction on a substrate, and having a predetermined portion being bent angularly and inwardly; a gate electrode projecting from one portion of the gate line; a gate insulating layer on an entire surface of the substrate; a data line being overlapped with some of the bent portion of the gate line, the data line for being in perpendicular to the gate line to define a pixel region; a source electrode projecting from the data line; a drain electrode on the gate insulating layer at a fixed interval from the source electrode; an active layer below the data line, the source electrode and the drain electrode; and a pixel electrode in the pixel region.

[TYPICAL DRAWINGS]

FIG. 4

[INDEX]

gate line, gate electrode, curved line

[SPECIFICATION]

[TITLE OF THE INVENTION]

LIQUID CRYSTAL DISPLAY DEVICE AND METHOD FOR
FABRICATING THE SAME

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[BRIEF DESCRIPTION OF THE DRAWINGS]

FIG. 1 is an enlarged plan view illustrating a unit pixel region of an LCD device according to the related art.

FIG. 2 is an enlarged plan view illustrating a unit pixel region of an LCD device according to the first embodiment of the present invention.

FIG. 3A to FIG. 3C are cross-sectional views illustrating manufacturing process steps of an LCD device according to the first embodiment of the present invention.

FIG. 4 is an enlarged plan view illustrating a unit pixel region of an LCD device according to the second embodiment of the present invention.

FIG. 5A to FIG. 5C are cross-sectional views illustrating manufacturing process steps of an LCD device according to the second embodiment of the present invention.

FIG. 6 is an enlarged plan view illustrating a unit pixel region of an LCD device according to the third embodiment of the present invention.

Description of reference numerals for main parts in the drawings

21, 41, 61: gate line	21a, 41a, 61a: gate electrode
22, 42, 62: data line	22a, 42a, 62a: source electrode
22b, 42b, 62b: drain electrode	22c, 42c, 62c: storage upper electrode
23, 43, 63: active layer	24a, 44a, 64a: first contact hole

24b, 44b, 64b: second contact hole

25, 45, 65: pixel electrode

[DETAILED DESCRIPTION OF THE INVENTION]

[OBJECT OF THE INVENTION]

5 [FIELD OF THE INVENTION AND DISCUSSION OF THE RELATED ART]

The present invention relates to a liquid crystal display (LCD) device, and more particularly, to an LCD device and a method for manufacturing the same, in which structures of a gate electrode and a gate line are changed, so that it is possible to prevent a data line and a drain electrode from being open at crossing areas (step difference)
10 being overlapped with the gate line and the gate electrode, respectively.

With development of information society, demands for various display devices increase. Accordingly, many efforts have been made to research and develop various flat display devices such as liquid crystal display (LCD), plasma display panel (PDP), electroluminescent display (ELD), and vacuum fluorescent display (VFD), and some
15 species of the flat display devices are already applied to displays of various equipments.

Among the various flat display devices, the liquid crystal display (LCD) device has been most widely used due to advantageous characteristics of thinness, lightness in weight, and low power consumption, whereby the LCD device substitutes for Cathode Ray Tube (CRT). In addition to the mobile type LCD devices such as a display for a
20 notebook computer, the LCD devices have been developed for computer monitors and televisions to receive and display broadcasting signals.

Despite various technical developments in the LCD technology with applications in different fields, research in enhancing the picture quality of the LCD device has been in some respects lacking as compared to other features and advantages

of the LCD device. In order to use the LCD device in various fields as a general display, the key to developing the LCD device lies on whether the LCD device can implement a high quality picture, such as high resolution and high luminance with a large-sized screen while still maintaining lightness in weight, thinness, and low power consumption.

The LCD device includes an LCD panel for displaying a picture image, and a driving part for applying a driving signal to the LCD panel. The LCD panel includes lower and upper substrates bonded to each other at a predetermined interval, and a liquid crystal layer injected between the lower and upper substrates.

The lower substrate (TFT array substrate) includes a plurality of gate and data lines, a plurality of pixel electrodes, and a plurality of thin film transistors. At this time, the plurality of gate lines are formed on the first glass substrate at fixed intervals in one direction, and the plurality of data lines are formed at fixed intervals in perpendicular to the plurality of gate lines. Then, the plurality of pixel electrodes of a matrix arrangement are respectively formed in pixel regions defined by the plurality of gate and data lines crossing each other. The plurality of thin film transistors are switched according to signals of the gate lines for transmitting signals of the data lines to the respective pixel electrodes.

The upper substrate (color filter substrate) includes a black matrix layer excluding light from regions except the pixel regions of the first substrate, R/G/B color filter layer displaying various colors, and a common electrode displaying the picture image.

Next, a predetermined space is maintained between the lower and upper substrates by spacers, and the lower and upper substrates are bonded to each other by a

sealant. Then, the liquid crystal layer is formed in the inner space of the sealant. When manufacturing the LCD device having the aforementioned structure, a plurality of LCD panels are formed on one large substrate in due consideration of sizes of the LCD panel and the substrate, simultaneously.

5 More specifically, an LCD device according to the related art will be described as follows.

FIG. 1 is an enlarged plan view illustrating a unit pixel region of an LCD device according to the related art. As shown in FIG. 1, a gate line 1 is formed at a fixed interval in one direction on a lower substrate (not shown), and a gate electrode 1a is projecting from the gate line 1 in one direction. At this time, a storage lower electrode of a storage capacitor is formed in one body as the preceding gate line 1. That is, the preceding gate line 1 serves as the storage lower electrode.

Then, a gate insulating layer (not shown) is formed on the lower substrate including the gate line 1 and the gate electrode 1a, and a data line 2 is formed on the gate insulating layer for being in perpendicular to the gate line 1, thereby defining a pixel region. Subsequently, a source electrode 2a is projecting from the data line 2, and a drain electrode 2b is formed at a fixed interval from the source electrode 2a. At this time, the source electrode 2a is formed in a 'C'-shaped hollow, and the drain electrode 2b is formed inside the 'C'-shaped hollow for being apart from the source electrode 2a at the fixed interval, whereby a 'C'-shaped channel region is defined between the source electrode 2a and the drain electrode 2b.

Next, an active layer 3 having a predetermined shape is patterned on the gate insulating layer. In this state, the active layer 3 is formed below the data line 2, the source electrode 2a and the drain electrode 2b to have a size enough for covering the

data line 2, the source electrode 2a and the drain electrode 2b. That is, the size of the active layer 3 is larger than a size including the data line 2, the source electrode 2a and the drain electrode 2b. The active layer 3 is formed in a method of sequentially depositing an amorphous silicon layer and n^+ amorphous silicon layer. Then, a storage upper electrode 2c is formed at one portion of the preceding gate line 1 serving as the storage lower electrode.

After that, a passivation layer (not shown) is formed on an entire surface of the lower substrate, the passivation layer having a first contact hole 4a at one portion of the drain electrode 2b, and a second contact hole 4b at one portion of the storage upper electrode 2c. Then, a pixel electrode 5 is formed in the pixel region for being in contact with the drain electrode 2b through the first contact hole 4a, and for being in contact with the storage upper electrode 2c through the second contact hole 4b. Subsequently, a conductive layer is deposited on the gate insulating layer, and then a wet-etch process is performed thereto, thereby forming the data line 2, the source electrode 2a and the drain electrode 2b.

However, the LCD device and the method for manufacturing the same according to the related art have the following disadvantages.

When the gate electrode 1a is shifted, an overlapped crossing area between the gate line 1 and the data line 2 is changed, whereby signal distortion may be generated by Cgd change. Also, as shown in 'A' region of FIG. 1, when patterning the data line, the source electrode and the drain electrode by the wet-etch process, the crossing area (step difference) between the gate line 1 and the data line 2 has a narrow width (arrow \leftrightarrow). As a result, the data line 2 of the crossing area may be corroded by an etchant, thereby generating disconnection of the lines.

Furthermore, as shown in 'B' region of FIG. 1, since an overlap area (step difference) between the gate electrode 1a and the drain electrode 2b has a narrow width (arrow \leftrightarrow), the drain electrode 2b of the overlap area may be corroded by the etchant, thereby generating disconnection.

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[TECHNICAL TASKS TO BE ACHIEVED BY THE INVENTION]

Accordingly, the present invention is directed to a liquid crystal display device and a method for manufacturing the same that substantially obviates one or more problems due to limitations and disadvantages of the related art.

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An object of the present invention is to provide a liquid crystal display device and a method for manufacturing the same, in which structures of a gate electrode and a gate line are changed, so that it is possible to prevent a data line and a drain electrode from being open at crossing areas (step difference) overlapped with the gate line and the gate electrode, respectively.

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Another object of the present invention is to provide a liquid crystal display device and a method for manufacturing the same, which prevents signal distortion by minimizing Cgd change.

[PREFERRED EMBODIMENTS OF THE INVENTION]

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To achieve these objects and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, an LCD device includes a gate line arranged at one direction on a substrate, and having a predetermined portion being bent angularly and inwardly; a gate electrode projecting from one portion of the gate line; a gate insulating layer on an entire surface of the substrate; a data line

being overlapped with some of the bent portion of the gate line, the data line for being in perpendicular to the gate line to define a pixel region; a source electrode projecting from the data line; a drain electrode on the gate insulating layer at a fixed interval from the source electrode; an active layer below the data line, the source electrode and the drain electrode; and a pixel electrode in the pixel region.

Also, the active layer is overlapped with an upper side of the gate electrode, and predetermined portions of the source and drain electrodes.

In another aspect, an LCD device includes a gate line arranged at one direction on a substrate, and having a predetermined portion being bent angularly and inwardly; a gate electrode projecting from one portion of the gate line, and having a predetermined portion being bent angularly and inwardly; a gate insulating layer on an entire surface of the substrate; a data line being overlapped with some of the bent portion of the gate line, and being in perpendicular to the gate line to define a pixel region; a source electrode projecting from the data line; a drain electrode formed at a fixed interval from the source electrode for being overlapped with the bent portion of the gate electrode; an active layer below the data line, the source electrode and the drain electrode; and a pixel electrode in the pixel region.

At this time, the bent portion of the gate line is formed in a curved line.

Also, the bent portion of the gate electrode is formed in a curved line.

In another aspect, a method for manufacturing an LCD device includes forming a gate line arranged at one direction on a substrate, and having a predetermined portion being bent angularly and inwardly; forming a gate electrode projecting from one portion of the gate line; sequentially depositing a gate insulating layer, a semiconductor layer and a conductive layer on the substrate including the gate line; forming a data line being

overlapped with some of the bent portion of the gate line, and being in perpendicular to the gate line by etching the conductive layer, thereby defining a pixel region; forming a source electrode projecting from the data line; forming a drain electrode at a fixed interval from the source electrode on the gate insulating layer; forming an active layer by etching the semiconductor layer with the data line, the source electrode and the drain electrode as a mask; and forming a pixel electrode in the pixel region.

At this time, the gate electrode is projecting from one portion of the gate line, and a predetermined portion of the gate electrode is bent angularly and inwardly.

Also, the drain electrode is overlapped with some of the bent portion of the gate electrode.

Hereinafter, an LCD device and a method for manufacturing the same according to the preferred embodiments of the present invention will be described as follows. In the LCD device according to the present invention, pattern shapes and structures of a gate electrode and a gate line are changed for preventing a data line from being open at a crossing area between gate and data lines, and a drain electrode from being open at an overlap area between gate and drain electrodes.

First embodiment

FIG. 2 is an enlarged plan view illustrating a unit pixel region of an LCD device according to the first embodiment of the present invention. FIG. 3A to FIG. 3C are cross-sectional views illustrating manufacturing process steps of an LCD device according to the first embodiment of the present invention.

As shown in FIG. 2 illustrating the unit pixel region of the LCD device according to the first embodiment of the present invention, a gate line 21 is arranged at a fixed interval in one direction on a transparent lower substrate (not shown), and a gate

electrode 21a is projecting from the gate line 21 in one direction. At this time, a storage lower electrode of a storage capacitor is formed in one body as the preceding gate line 21. That is, the preceding gate line 21 serves as the storage lower electrode. Then, a gate insulating layer (not shown) is formed on the transparent lower substrate including the gate line 21 and the gate electrode 21a. Also, a data line 22 is formed on the gate insulating layer for being in perpendicular to the gate line 21, thereby defining a pixel region.

At this time, the gate line 21 is bent angularly and inwardly at a lower crossing boundary (step difference) between the gate and data lines 21 and 22. The gate line 21 may be formed in a curved line at the lower crossing boundary (step difference). On comparing 'C' region of FIG. 2 to 'A' region of FIG. 1, it is shown definitely that the lower crossing boundary between the gate and data lines 21 and 22 in the unit pixel of the LCD device according to the present invention is longer than that according to the related art. At this time, in the portion of the gate line 21 being bent angularly and inwardly, some parts are overlapped with the data line 22, and the rest are not overlapped with the data line 22.

In the aforementioned structure of the LCD device, even though the gate electrode 21a is shifted, it is possible to compensate the crossing area between the gate and data lines 21 and 22 by the bent portion of the lower crossing boundary (step difference), thereby minimizing entire Cgd changes. Also, a source electrode 22a is projecting from the data line 22, and a drain electrode 22b is formed at a fixed interval from the source electrode 22a. In this case, the source electrode 22a is formed in a 'C'-shaped hollow, and the drain electrode 22b is formed inside the 'C'-shaped hollow for being apart from the source electrode 22a at the fixed interval, whereby a 'C'-

shaped channel region is defined between the source electrode 22a and the drain electrode 22b.

Also, an active layer 23 having a predetermined shape is patterned on the gate insulating layer. In this state, the active layer 23 is formed below the data line 22, the source electrode 22a and the drain electrode 22b in a size enough for covering the data line 22, the source electrode 22a and the drain electrode 22b. That is, the size of the active layer 23 is larger than a size including the data line 22, the source electrode 22a and the drain electrode 22b. The active layer 23 is formed in a method of sequentially depositing an amorphous silicon layer and n^+ amorphous silicon layer. Then, a storage upper electrode 22c is formed at one portion of the preceding gate line 21 serving as the storage lower electrode.

Next, a passivation layer (not shown) is formed on an entire surface of the transparent lower substrate, the passivation layer having a first contact hole 24a at one portion of the drain electrode 22b, and a second contact hole 24b at one portion of the storage upper electrode 22c. Then, a pixel electrode 25 is formed in the pixel region for being in contact with the drain electrode 22b through the first contact hole 24a, and for being in contact with the storage upper electrode 22c through the second contact hole 24b. At this time, the data line 22 is formed of one of metal materials such as chrome Cr, molybdenum Mo, titanium Ti and tantalum Ta, or is formed of one of molybdenum Mo alloys such as MoW, MoTa and MoNo. The passivation layer 22 is formed of an inorganic insulating material such as Si_3N_4 or oxide silicon SiO_2 , or an organic insulating material such as acrylic organic compound, Teflon, Benzocyclobuten BCB, Cytop or Perfluorocyclobutane PFCB. Also, the pixel electrode 25 is formed of

any one of Indium-Tin-Oxide ITO, Indium-Zinc-Oxide IZO, and Indium-Tin-Zinc-Oxide ITZO.

A method for manufacturing the aforementioned LCD device according to the first embodiment of the present invention will be described as follows.

5 As shown in FIG. 3A, one of conductive metal materials such as chrome Cr, aluminum Al, aluminum alloy AlNd, tantalum Ta and molybdenum Mo is deposited on the lower substrate (not shown), and then a patterning process is performed thereon with a first mask by photolithography, thereby forming the gate line 21 arranged at one direction, and the gate electrode 21a projecting from the gate line 21 at one direction.

10 At this time, the gate line 21 is inwardly bent at the lower crossing boundary (step difference) between the gate line 21 and the data line 25, so that the lower crossing boundary becomes longer. As a result, it is possible to prevent the data line from being corroded at the crossing area (step difference) being overlapped with the gate line 21 by an etchant, thereby preventing disconnection of the lines. Further, the gate line 21 may

15 be formed in a curved line at the lower crossing boundary.

 The conductive metal layer may have a dual-layered structure having lower and upper layers. For example, the lower layer of the conductive metal layer is formed of Al or AlNd, and the upper layer of the conductive metal layer is formed of Mo. Or, the lower layer of the conductive metal layer is formed of Cr, and the upper layer of the

20 conductive metal layer is formed of AlNd. After that, the gate insulating layer (not shown) is formed on the entire surface of the lower substrate including the gate line 21.

 Referring to FIG. 3B, the amorphous silicon layer (not shown) and n^+ amorphous silicon layer (not shown) are sequentially deposited on the gate insulating layer for forming the active layer. Then, another conductive layer is formed on the

entire surface of the lower substrate. At this time, the conductive layer is formed of the metal material such as chrome Cr, molybdenum Mo, titanium Ti or tantalum Ta, or is formed of any one of the molybdenum Mo alloys such as MoW, MoTa and MoNo. After that, a wet-etch process is performed to the conductive layer by using a second
5 mask, thereby forming the data line 22, the source electrode 22a, the drain electrode 22b and the storage upper electrode 22c. In this state, the second mask is patterned in a half tone at a portion corresponding to the channel region. Next, a dry-etch process is performed to the amorphous silicon layer and n^+ amorphous layer by using the data line 22, the source electrode 22a and the drain electrode 22b as a mask, thereby forming the
10 active layer 23. Then, the n^+ amorphous silicon layer in the channel region is removed by ashing, thereby forming an ohmic contact layer.

At this time, the source electrode 22a is formed in the 'C'-shaped hollow on the gate electrode 21a, and the drain electrode 22b is formed inside the 'C'-shaped hollow on one portion of the gate electrode 21a at the fixed interval from the source
15 electrode 22a. In this process, the 'C'-shaped channel region is formed between the source electrode 22a and the drain electrode 22b, and the active layer 23 has the size larger than the size including the data line 2, the source electrode 21 and the drain electrode 2b.

Although not shown, the passivation layer is formed on the lower substrate.
20 At this time, the passivation layer is formed of the inorganic insulating material such as Si_3N_4 or oxide silicon SiO_2 , or the organic insulating material such as acrylic organic compound, Teflon, Benzocyclobuten BCB, Cytop or Perfluorocyclobutane PFCB. After that, a photoresist layer (not shown) is deposited on the passivation layer, and then selectively patterned by exposure and developing process. At this time, the photoresist

layer is patterned to expose the passivation layer above the drain electrode 22b and the storage upper electrode 22c of the preceding gate line 21.

As shown in FIG. 3C, the passivation layer is etched by using the patterned photoresist layer as a mask (third mask), thereby forming the first contact hole 24a at one direction of the drain electrode 22b, and the second contact hole 24b at one direction of the storage upper electrode 22c of the preceding gate line 21. Then, a transparent electrode is deposited on the lower substrate, and then the photolithography process using a fourth mask is performed thereto, thereby forming the pixel electrode 25 in the pixel region including the first and second contact holes 24a and 24b. At this time, the pixel electrode 25 is formed of any one of Indium-Tin-Oxide ITO, Indium-Zinc-Oxide IZO, and Indium-Tin-Zinc-Oxide ITZO.

Second embodiment

FIG. 4 is an enlarged plan view illustrating a unit pixel region of an LCD device according to the second embodiment of the present invention. FIG. 5A to FIG. 5C are cross-sectional views illustrating manufacturing process steps of an LCD device according to the second embodiment of the present invention. In addition to the structure of the LCD device according to the first embodiment of the present invention, a gate electrode has a predetermined portion being bent inwardly to increase an overlap boundary (step difference) between gate and drain electrodes.

Hereinafter, an LCD device according to the second embodiment of the present invention will be described as follows.

As shown in FIG. 4 illustrating the unit pixel region of the LCD device according to the second embodiment of the present invention, a gate line 41 is arranged at a fixed interval in one direction on a transparent lower substrate (not shown), and a

gate electrode 41a is projecting from the gate line 41 in one direction. At this time, a storage lower electrode of a storage capacitor is formed in one body as the preceding gate line 41. That is, the preceding gate line 41 serves as the storage lower electrode. Then, a gate insulating layer (not shown) is formed on the transparent lower substrate including the gate line 41 and the gate electrode 41a. Also, a data line 42 is formed on the gate insulating layer for being in perpendicular to the gate line 41, thereby defining a pixel region. After that, a source electrode 42a is projecting from the data line 42, and a drain electrode 42b is formed at a fixed interval from the source electrode 42a. At this time, the source electrode 42a is formed in a 'C'-shaped hollow, and the drain electrode 42b is formed inside the 'C'-shaped hollow at the fixed interval from the source electrode 42a.

At this time, the gate line 41 is bent angularly and inwardly at a lower crossing boundary (step difference) between the gate and data lines 41 and 42. The gate line 41 may be formed in a curved line at the lower crossing boundary (step difference). On comparing 'C' region of FIG. 4 to 'A' region of FIG. 1, it is shown definitely that the lower crossing boundary between the gate and data lines 41 and 42 in the unit pixel of the LCD device according to the present invention is longer than that according to the related art. At this time, in the portion of the gate line 41 being bent angularly and inwardly, some parts are overlapped with the data line 42, and the rest are not overlapped with the data line 42. In the aforementioned structure of the LCD device, even though the gate electrode 41a is shifted, it is possible to compensate the crossing area between the gate and data lines 41 and 42 by the bent portion of the lower crossing boundary (step difference), thereby minimizing entire Cgd change.

Also, the gate electrode 41a has a predetermined portion being bent angularly and inwardly at an overlap boundary (step difference) between the gate electrode 41a and the drain electrode 42b. Accordingly, the overlap boundary (step difference) between the gate electrode 41a and the drain electrode 42b in the unit pixel region of the LCD device according to the present invention is longer than that according to the related art. It is shown definitely when comparing 'D' region of FIG. 4 to 'B' region of FIG. 1. Further, the bent portion of the gate electrode 41a may be formed in a curved line.

Then, a 'C'-shaped channel region is defined between the source electrode 42a and the drain electrode 42b. Also, an active layer 43 having a predetermined shape is patterned on the gate insulating layer. In this state, the active layer 43 is formed below the data line 42, the source electrode 42a and the drain electrode 42b in a size enough for covering the data line 42, the source electrode 42a and the drain electrode 42b. That is, the size of the active layer 43 is larger than a size including the data line 42, the source electrode 42a and the drain electrode 22b. The active layer 43 is formed in a method of sequentially depositing an amorphous silicon layer and n^+ amorphous silicon layer. Then, a storage upper electrode 42c is formed at one portion of the preceding gate line 41 serving as the storage lower electrode.

Next, a passivation layer (not shown) is formed on an entire surface of the lower substrate, the passivation layer having a first contact hole 44a at one portion of the drain electrode 42b, and a second contact hole 44b at one portion of the storage upper electrode 42c. Then, a pixel electrode 45 is formed in the pixel region for being in contact with the drain electrode 42b through the first contact hole 44a, and for being in contact with the storage upper electrode 42c through the second contact hole 44b.

At this time, the data line 42 is formed of one of metal materials such as chrome Cr, molybdenum Mo, titanium Ti and tantalum Ta, or is formed of one of molybdenum Mo alloys such as MoW, MoTa and MoNb. The passivation layer 42 is formed of an inorganic insulating material such as Si_3N_4 or oxide silicon SiO_2 , or an organic
5 insulating material such as acrylic organic compound, Teflon, Benzocyclobuten BCB, Cytop or Perfluorocyclobutane PFCB. Also, the pixel electrode 45 is formed of any one of Indium-Tin-Oxide ITO, Indium-Zinc-Oxide IZO, and Indium-Tin-Zinc-Oxide ITZO.

A method for manufacturing the aforementioned LCD device according to the
10 second embodiment of the present invention will be described as follows.

As shown in FIG. 5A, one of conductive metal materials such as chrome Cr, aluminum Al, aluminum alloy AlNd, tantalum Ta and molybdenum Mo is deposited on the lower substrate (not shown), and then a patterning process is performed thereon with a first mask by photolithography, thereby forming the gate line 41 arranged at one
15 direction, and the gate electrode 41a projecting from the gate line 41 at one direction. At this time, the gate line 41 is angularly and inwardly bent at the lower crossing boundary (step difference) between the gate line 41 and the data line 45, so that the lower crossing boundary becomes longer. As a result, it is possible to prevent the data line 42 from being corroded at the crossing area (step difference) being overlapped with
20 the gate line 41 by an etchant, thereby preventing disconnection of the lines. Further, the gate line 41 may be formed in a curved line at the lower crossing boundary.

At this time, in the portion of the gate line 41 being bent angularly and inwardly, some parts are overlapped with the data line 42, and the rest are not overlapped with the data line 42. In the aforementioned structure of the LCD device,

even though the gate electrode 41a is shifted, it is possible to compensate the crossing area between the gate and data lines 41 and 42 by the bent portion of the lower crossing boundary (step difference), thereby minimizing entire Cgd change.

Also, the gate electrode 41a has the predetermined portion being bent angularly
5 and inwardly at the overlap boundary (step difference) between the gate electrode 41a and the drain electrode 42b. Accordingly, the overlap boundary (step difference) between the gate electrode 41a and the drain electrode 42b in the unit pixel region of the LCD device according to the present invention is longer than that according to the related art, whereby it is possible to prevent the drain electrode 42b from being corroded
10 at the overlap boundary (step difference) being overlapped with the gate electrode 41a by the etchant, thereby preventing disconnection. Furthermore, the bent portions of the gate line 41 and the gate electrode 41a may be formed in curved lines.

The conductive metal layer may have a dual-layered structure having lower and upper layers. For example, the lower layer of the conductive metal layer is formed of
15 Al or AlNd, and the upper layer of the conductive metal layer is formed of Mo. Or, the lower layer of the conductive metal layer is formed of Cr, and the upper layer of the conductive metal layer is formed of AlNd. After that, the gate insulating layer (not shown) is formed on the entire surface of the lower substrate including the gate line 41.

Hereinafter, the structures shown in FIG. 5B and FIG. 5C are same as those
20 according to the first embodiment of the present invention.

Third embodiment

FIG. 6 is an enlarged plan view illustrating a unit pixel region of an LCD device according to the third embodiment of the present invention. As shown in FIG. 6 illustrating the unit pixel region of the LCD device according to the third embodiment

of the present invention, a gate line 61 is formed at a fixed interval in one direction on a lower substrate (not shown), and a gate electrode 61a is projecting from the gate line 61 in one direction. Then, a storage lower electrode is formed in one body as the gate line 61, at a position corresponding to a storage capacitor of the preceding gate line.

5 At this time, the gate line 61 is bent angularly and inwardly at a lower crossing boundary (step difference) between the gate and data lines 61 and 62. That is, the lower crossing boundary between the gate and data lines 61 and 62 in the unit pixel of the LCD device according to the present invention is longer than that according to the related art. Thus, it is possible to prevent the data line 62 from being corroded at the
10 crossing area (step difference) overlapped with the gate line 61 by an etchant, thereby preventing disconnection of the lines. At this time, in the portion of the gate line 61 being bent angularly and inwardly, some parts are overlapped with the data line 62, and the rest are not overlapped with the data line 62.

 Although not shown, a gate pad is formed at one end of the gate line 61, and a
15 source pad is formed at one end of the data line 62. Also, a gate insulating layer (not shown) is formed on the lower substrate including the gate line 61, the gate electrode 61a and the storage lower electrode, for electrically insulating the gate line 61, the gate electrode 61a and the storage lower electrode from an upper layer. Then, an active layer 63 is formed on the gate insulating layer above the gate electrode 61a. At this
20 time, the active layer 63 is formed in a structure of sequentially depositing an amorphous silicon layer 63a and a doped amorphous silicon layer 63b.

 Then, the data line 62 is formed in perpendicular to the gate line 61, thereby forming a pixel region. Also, a source electrode 62a is projecting from the data line 62 in one direction for being overlapped with one side of the active layer 63, and a drain

electrode 62b is formed at a fixed interval from the source electrode 62a for being overlapped with the other side of the active layer 63. After that, a storage upper electrode 62c is formed above the storage lower electrode. Also, a passivation layer (not shown) is formed on the lower substrate, the passivation layer having first and second contact holes 64a and 64b corresponding to the drain electrode 62b and the storage upper electrode 62c. A pixel electrode 65 is formed in the pixel region for being in contact with the drain electrode 62b and the storage upper electrode 62c through the first and second contact holes 64a and 64b.

10 [ADVANTAGES OF THE INVENTION]

As mentioned above, the LCD device and method for manufacturing the same has the following advantages.

First, the gate line is bent angularly and inwardly at the lower crossing boundary (step difference) being overlapped with the data line, thereby increasing the lower crossing boundary between the gate and data lines. Thus, it is possible to prevent the data line from being open at the crossing area between the gate and data lines.

Also, a predetermined portion of the gate electrode overlapped with the drain electrode is bent angularly and inwardly, thereby increasing the overlap boundary between the gate and drain electrodes. Thus, it is possible to prevent the drain electrode from being open at the overlap area between the gate and drain electrodes.

Thus, the entire Cgd change is minimized even though the gate electrode is shifted, thereby preventing signal distortion.

It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

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What is claimed is:

1. An LCD device comprising:

- 5 a gate line arranged at one direction on a substrate, and having a predetermined portion being bent angularly and inwardly;
- a gate electrode projecting from one portion of the gate line;
- a gate insulating layer on an entire surface of the substrate;
- a data line being overlapped with some of the bent portion of the gate line, the data line for being in perpendicular to the gate line to define a pixel region;
- 10 a source electrode projecting from the data line;
- a drain electrode on the gate insulating layer at a fixed interval from the source electrode;
- an active layer below the data line, the source electrode and the drain electrode;
- and
- 15 a pixel electrode in the pixel region.

2. The LCD device of claim 1, wherein the active layer is overlapped with an upper side of the gate electrode, and predetermined portions of the source and drain electrodes.

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3. An LCD device comprising:

- a gate line arranged at one direction on a substrate, and having a predetermined portion being bent angularly and inwardly;
- a gate electrode projecting from one portion of the gate line, and having a

predetermined portion being bent angularly and inwardly;

a gate insulating layer on an entire surface of the substrate;

a data line being overlapped with some of the bent portion of the gate line, and
being in perpendicular to the gate line to define a pixel region;

5 a source electrode projecting from the data line;

a drain electrode formed at a fixed interval from the source electrode for being
overlapped with the bent portion of the gate electrode;

an active layer below the data line, the source electrode and the drain electrode;

and

10 a pixel electrode in the pixel region.

4. The LCD device of claim 1 or 3, wherein the bent portion of the gate line is
formed in a curved line.

15 5. The LCD device of claim 3, wherein the bent portion of the gate electrode is
formed in a curved line.

6. A method for manufacturing an LCD device comprising:

forming a gate line arranged at one direction on a substrate, and having a
20 predetermined portion being bent angularly and inwardly;

forming a gate electrode projecting from one portion of the gate line;

sequentially depositing a gate insulating layer, a semiconductor layer and a
conductive layer on the substrate including the gate line;

forming a data line being overlapped with some of the bent portion of the gate

line, and being in perpendicular to the gate line by etching the conductive layer, thereby defining a pixel region;

forming a source electrode projecting from the data line;

forming a drain electrode at a fixed interval from the source electrode on the
5 gate insulating layer;

forming an active layer by etching the semiconductor layer with the data line,
the source electrode and the drain electrode as a mask; and

forming a pixel electrode in the pixel region.

10 7. The method of claim 6, wherein the gate electrode is projecting from one
portion of the gate line, and a predetermined portion of the gate electrode is bent
angularly and inwardly.

8. The method of claim 6 or 7, wherein the drain electrode is overlapped with
15 some of the bent portion of the gate electrode.

9. The method of claim 6, wherein the bent portion of the gate line is formed in
a curved line.

20 10. The method of claim 6, wherein the bent portion of the gate electrode is
formed in a curved line.

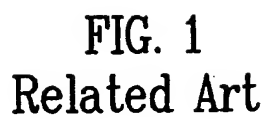
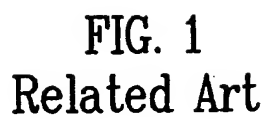


FIG. 2

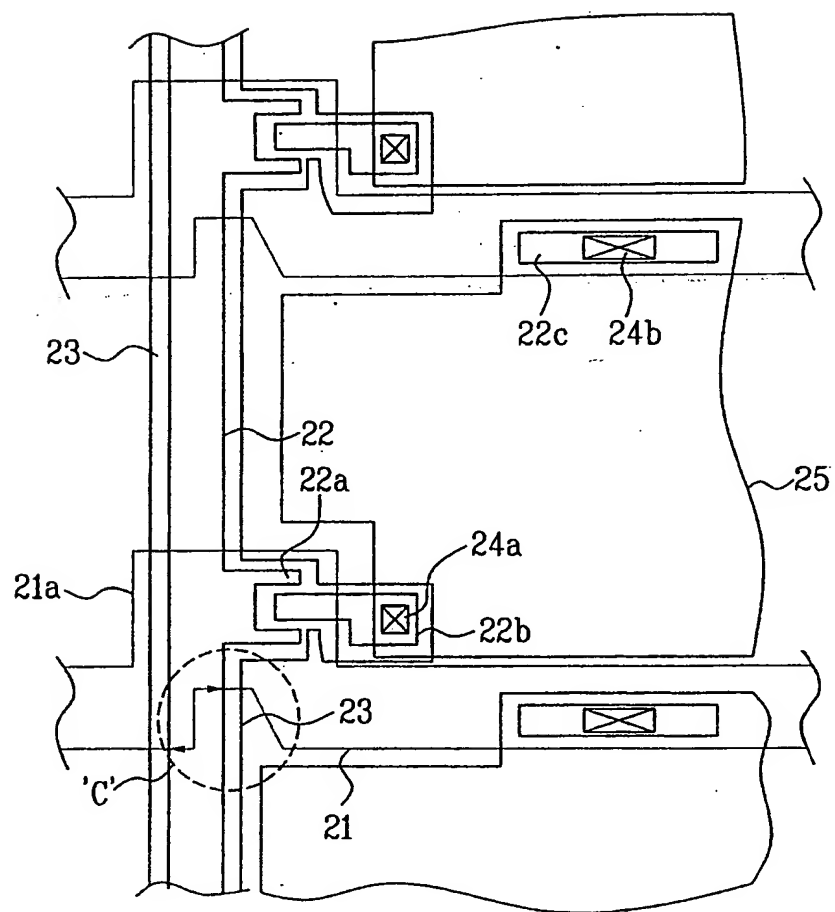


FIG. 3A

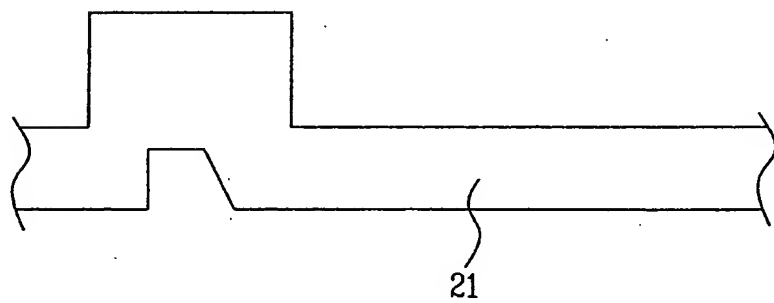
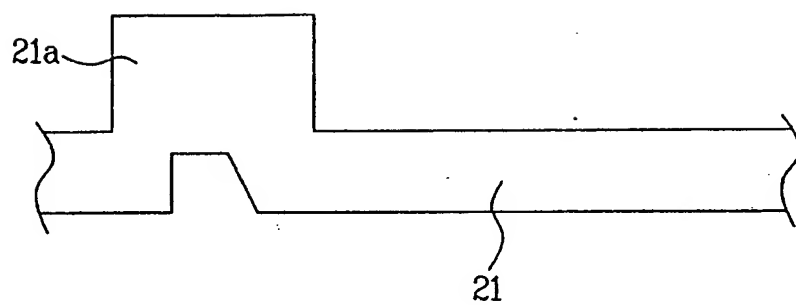


FIG. 3B

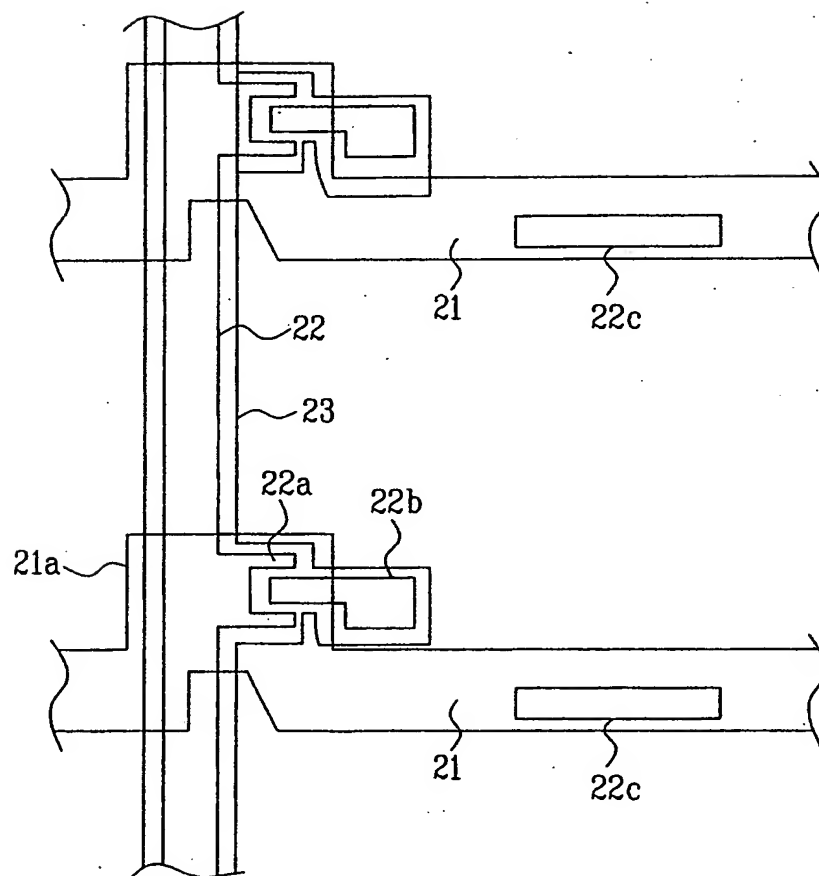


FIG. 3C

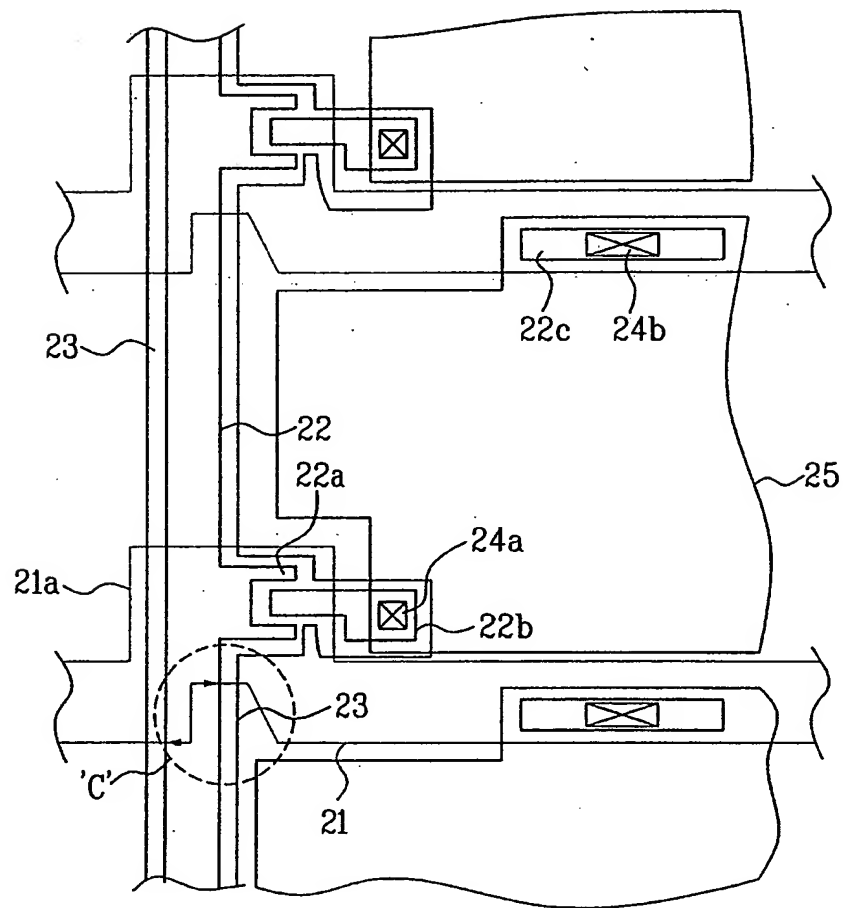


FIG. 4

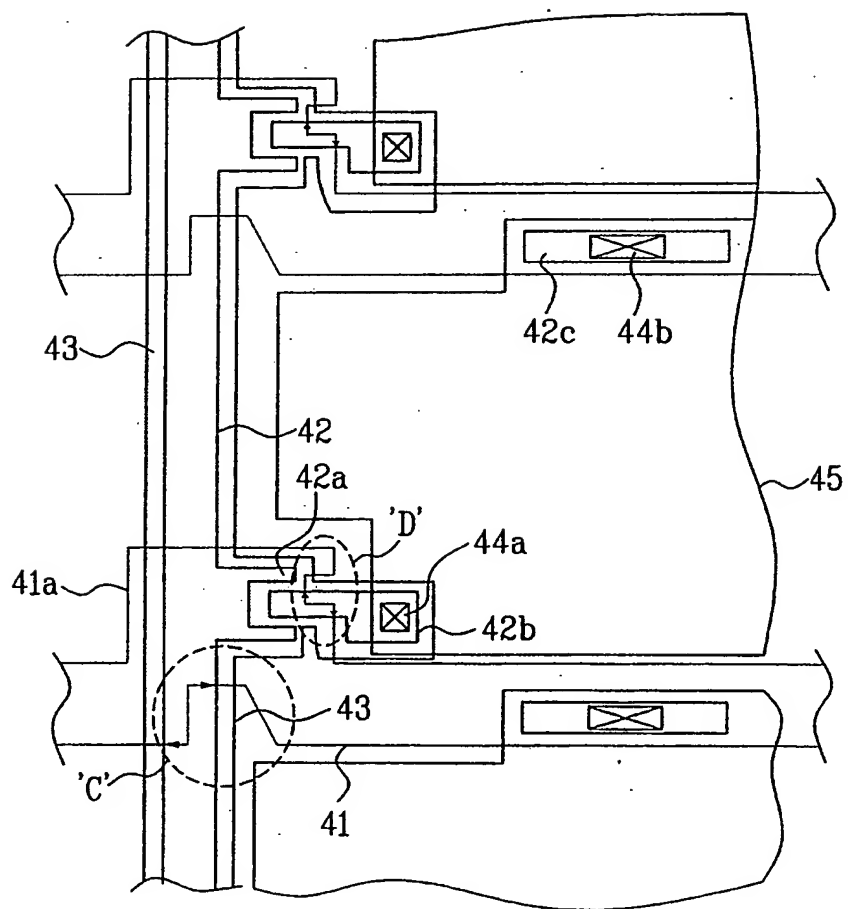


FIG. 5A

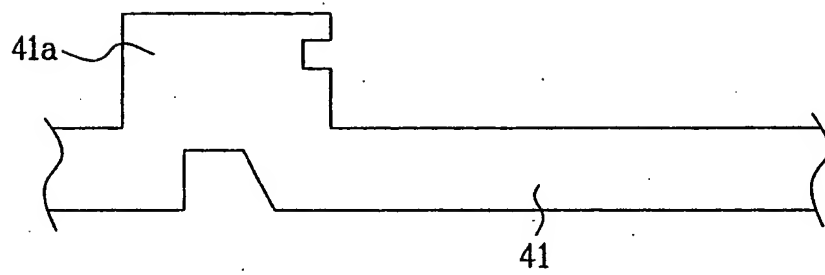
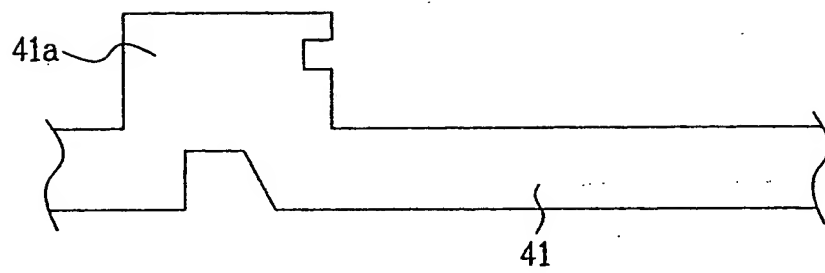


FIG. 5B

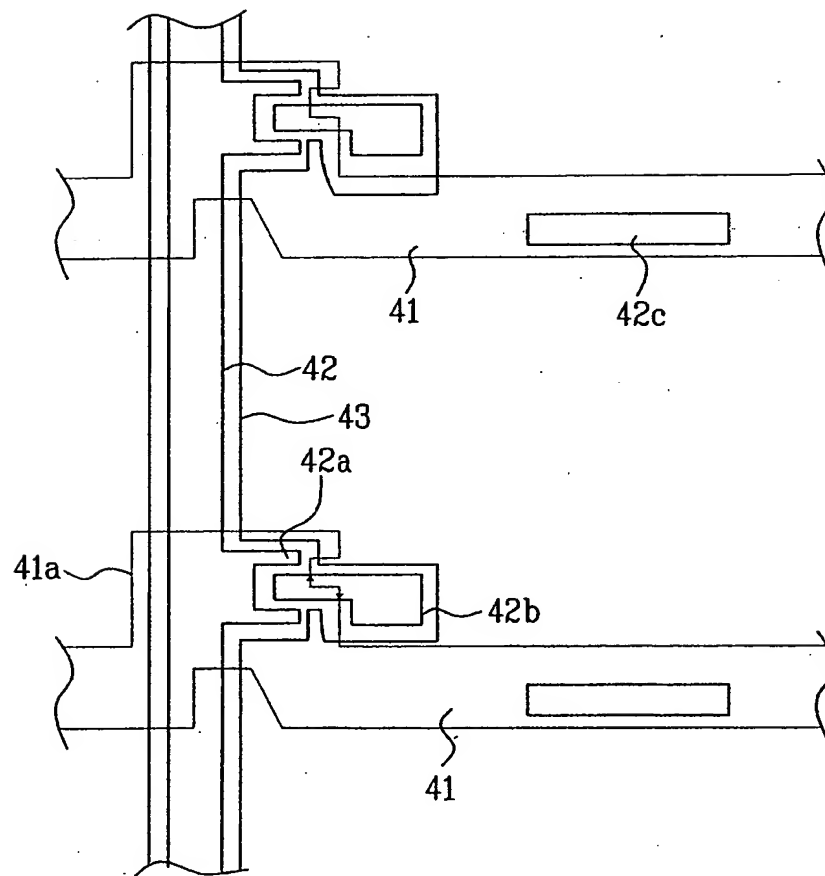


FIG. 5C

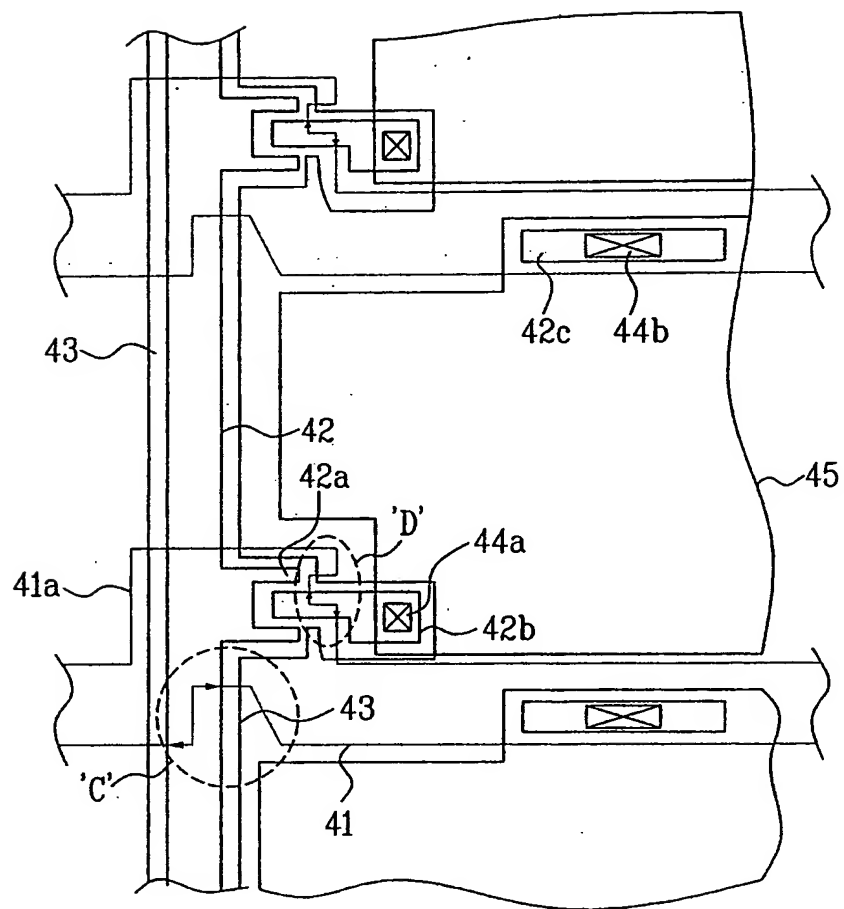


FIG. 6

